Curriculum Vitae

I. Educations

University		Degree	Study Period	Major
KAIST (Former ICU)		B.S.	02/24/2003 – 06/15/2006	Electrical Communications Engineering (IT-Engineering)
		M.S.	06/19/2006 – 02/14/2008	
University of Southern California (USC)		M.S.	08/27/2012 – 12/12/2018	Electrical Engineering (ElectroPhysics)
		Ph.D.	08/27/2012 – 08/06/2019	
Thesis Title	M.S.	Systematic power optimizing cyclic ADC design		
	Ph.D.	Energy-efficient design techniques and architectures for high-speed (GS/s) analog-to-digital converters		

II. Experience and Employment

Organization	Duration	Position	Activities and Responsibility	Location
ETRI	10/18/2006 – 10/17/2007	Part-time Researcher	CMOS low-power ADC design (ADC Architecture Development)	Daejeon, South Korea
	02/01/2008 – 06/18/2018 Leave of absence for Ph.D. degree (06/19/2012 – 06/18/2018)	Full-time Researcher	Sensor interface circuit design (Image/Audio/Display AFE)	Daejeon, South Korea
USC	08/25/2014 – 12/05/2014	Teaching Assistant	Mixed-Signal Integrated Circuit Design (EE536B)	Los Angeles, CA, US
	01/08/2017 – 04/27/2017			
Intel corporation	09/18/2017 – 12/29/2017	Intern	Next generation PCIe I/O PHY transceiver development	Santa Clara, CA, US
	09/23/2019 – 07/24/2020	Analog Engineer	Design wireline I/O circuits in Intel's leading-edge technology node	Hillsboro, OR, US
SeoulTech	**09/01/2020 – Present**	**Assistant Professor**	**Electronic Engineering (Mixed Signal Analog Circuit Design)**	**Seoul, South Korea**

III. Honor and Award

Date	Type	Organization
04/17/2019	Outstanding student paper award (3rd place)	IEEE-CICC
08/24/2006	President award (Graduate with honor)	KAIST
04/03/2009	President award (Outstanding researcher)	ETRI
02/27/2012	Scholarship: Ph.D. Fellowship	USC Viterbi School of Engineering

IV. Academic Achievements

a) Journal and conference papers

	Authors, Title, journal, Vol., page, and Year	# of Authors	Role	Type	Note
J 23	C.T. Ngo, H. W. Ko, J. W. Choi, **J.-W. Nam**, J.-P. Hong, "A lightweight and high yield CMOS TRNG with lightweight Photon post-processing," Sensors, vol. 24, no. 2702, pp. 1-13.	5	Co-Author	SCIE (IF=3.4)	Collaboration with CNBU
J 22	J.-Y. Park, **J.-W. Nam**, "A 4.3 GS/s time-interleaved ΔΣ DAC for qubit control," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol 71, no. 11, pp. 4663-4667.	2	Corresponding Author	SCIE (IF=4.4)	NRF-2022 R1A4A3029433
J 21	S. M. Kim, Y. Jeong, **J.-W. Nam**, "Solving Optimal EV Chargers Deployment Problem", Applied sciences, vol. 14, no. 5092, pp. 1-19.	3	Corresponding Author	SCIE	
J 20	V. K. Pham, C. T. Ngo, **J.-W. Nam**, J.-P. Hong, "A reconfigurable SRAM CRP PUF with high reliability and randomness", Electronics, vol. 14, no. 5092, pp. 1-19.	4	Co-Author	SCIE (IF=2.9)	Collaboration with CNBU
J 19	J.-Y. Park, S.-Y. Kim, H. Yoo, *__J.-W. Nam__ "Analysis of quarter method applied ROM-based DDFS architecture," IEEE ACCESS, vol. 11, pp. 117137-117148, Oct. 2023.	4	Corresponding Author	SCIE (IF=3.9)	NRF-2022 R1A4A3029433
J 18	D. Kim, J.-P. Hong, J. Lee, *__J.-W. Nam__, "High-speed light detection sensor for hardware security in standard CMOS technology," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol 40, no. 10, pp. 3917-3921, Oct. 2023.	4	Corresponding Author	SCIE (IF=4.4)	Collaboration with HYU

J 17	J.-W. Hyun, *<u>**J.-W. Nam**</u>, “AMS Circuit Design Optimization Technique Based on ANN Regression Model with VAE Structure,” IEEE ACCESS, vol. 11, pp. 58850-58862, Jun. 2023.	2	Corresponding Author	SCIE (IF=3.9)	
J 16	J. Kim, J. Han, *<u>**J.-W. Nam**</u>, *K, Cho, “CMOS interconnect electronics architecture for reliable and scalable quantum computer,” Journal of IKEEE, vol. 27, no. 1, pp. 12-18, 2023.	4	Co-Corresponding Author	KCI	NRF-2022 R1A4A3029433
C 15	H.-C. Lee, H.-J. Lee, J. Yoo, *<u>**J.-W. Nam**</u>, “Loss analysis and modeling of asynchronous buck-converter”, Summer annual conference of IEIE, Jeju, Jun. 2022.	4	Corresponding Author	Domestic Conference	Poster Presentation
C 14	D. Kim, H. Yoo, *<u>**J.-W. Nam**</u>, “Implementation of low-cost linear CMOS temperature sensor for biomedical application”, Summer annual conference of IEIE, Jeju, Jun. 2022.	3	Corresponding Author	Domestic Conference	Poster Presentation
C 13	J. Yoo, <u>**J.-W. Nam**</u>, J.-P. Hong, “Study on discard-rate of SRAM-based PUF”, Summer annual conference of IEIE, Jeju, Jun. 2022.	3	Co-Author	Domestic Conference	Poster Presentation
J 15	<u>**J.-W. Nam**</u>, J. Kim, and J.-P. Hong, “Stochastic Cell- and Bit-Discard Technique to Improve Randomness of a TRNG,” MDPI Electronics, vol. 11, no. 11, June 2022.	3	First Author	SCIE (IF=2.69)	Collaboration with CNBU
J 14	<u>**J.-W. Nam**</u>, J.-H. Ahn, and J.-P. Hong, "Compact SRAM-based PUF Chip Employing Body Voltage Control Technique," IEEE ACCESS, vol. 10, pp. 22311-22319, Feb. 2022.	3	First Author	SCIE (IF=3.476)	Collaboration with CNBU
J 13	<u>**J.-W. Nam**</u>, Y.-K. Cho and Y. K. Lee, "Regression Model-Based AMS Circuit Optimization Technique Utilizing Parameterized Operating Condition," MDPI Electronics, vol. 11, no. 3, Jan. 2022.	3	First Author	SCIE (IF=2.69)	
J 12	Y.-K. Cho, <u>**J.-W. Nam**</u>, S.-W. Lee, "A Low-Power Class-C Voltage-Controlled Oscillator with Robust Start-Up and Compact High-Q Capacitor Array," IEEE Trans. Circuits Syst. II, Exp. Briefs, Oct. 2021.	3	Co-Author	SCIE (IF=3.292)	Collaboration with KNU
J 11	Y.-K. Cho, <u>**J.-W. Nam**</u>, "Three-Dimensional Selective Oxidation Fin Channel MOSFET Based on Bulk Silicon Wafer," Journal of Convergence for Information Technology, vol. 11, no. 11, pp. 159-165, Nov. 2021.	2	Corresponding Author	KCI	Collaboration with KNU
J 10	<u>**J.-W. Nam**</u>, Y.-K. Cho, "5-bit FLASH A/D Converter Employing Time-interpolation Technique," Journal of Convergence for Information Technology, vol. 11, no. 9, pp. 124-129, Sept. 2021.	2	First Author	KCI	
C 12	S. Park, <u>**J.-W. Nam**</u>, and S. K. Gupta, “HW-BCP: A custom hardware accelerator for SAT suitable for single chip implementation for large benchmarks,” the 26th Asia and South Pacific Design Automation Conf., Jan. 2021.	3	Co-Author	International Conference	Oral Presentation
C 11	H. W. Kwon, <u>**J.-W. Nam**</u>, and Y. K. Lee, “Generative adversarial attacks on fingerprint recognition systems,” the 35th International Conf. on Information and networking (ICOIN), Jan. 2021.	3	Co-Author	International Conference	
C 10	<u>**J.-W. Nam**</u>, and Y. K. Lee, “Machine-learning based analog and mixed-signal circuit design and optimization,” the 35th International Conf. on Information and networking (ICOIN), Jan. 2021.	2	Co-Author	International Conference	Poster Presentation
J9	<u>**J.-W. Nam**</u>, and M.-W. Chen, “A 12.8-Gbaud ADC-based Wireline Receiver with Embedded IIR Equalizer,” IEEE J. Solid-State Circuits, vol. 55, no. 3, pp. 557 – 567, Mar. 2020.	2	First Author	SCIE (IF=5.013)	
C9	<u>**J.-W. Nam**</u>, and M.-W. Chen, “A 12.8-Gbaud ADC-based NRZ/PAM4 Receiver with Embedded Tunable IIR Equalization Filter Achieving 2.43-pJ/b in 65nm CMOS,” IEEE Custom Integrated Circuits Conf., April. 2019.	2	First Author	International Conference	Outstanding Student paper Award
J8	<u>**J.-W. Nam**</u>, M. Hassanpourghadi, A. Zhang, and S.-W. M. Chen, “A 12-bit 1.6, 3.2, and 6.4 GS/s 4-b/cycle Time-Interleaved SAR ADC with Dual Reference Shifting and Interpolation,” IEEE J. Solid-State Circuits, vol. 53, no. 6, pp. 1765-1779, May 2018.	4	First Author	SCIE (IF=5.173)	
J7	<u>**J.-W. Nam**</u>, and S.-W. M. Chen, “An embedded passive gain technique for asynchronous SAR ADC achieving 10.2 ENOB 1.36-mW at 95-MS/s in 65 nm CMOS,” IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 63, no. 10, pp. 1628 - 1638, Oct. 2016.	2	First Author	SCIE (IF=2.407)	
C8	<u>**J.-W. Nam**</u>, M. Hassanpourghadi, A. Zhang, and S.-W. M. Chen, “A 12-bit 1.6 GS/s interleaved SAR ADC with dual reference shifting and Interpolation achieving 17.8 fJ/conv-step in 65nm CMOS,” in Proc. IEEE Symp. VLSI Circuits, Jun. 2016, pp.154–156.	4	First Author	International Conference	Oral Presentation

C7	**J.-W. Nam**, D. Chiong, and S.-W. M. Chen, "A 95-MS/s 11-bit 1.36-mW asynchronous SAR ADC with embedded passive gain in 65 nm CMOS," IEEE Custom Integrated Circuits Conf., Sep. 2013, pp. 1–4.	3	First Author	International Conference	Oral Presentation
C6	**J.-W. Nam**, M. Hassanpourghadi, A. Zhang, and S.-W. M. Chen, "Low-power High Dynamic-range ADC with over GHz Bandwidth using Cost-efficient Multi-bit/cycle SAR ADC," GOMATech 2018.	4	First Author	Government Conference	
C5	M. Hassanpourghadi, Q. Zhang, P. Sharma, **J.-W. Nam**, S. Su, S. Chowdhury, M.S.W. Chen, Sandeep Gupta, A.F.J. Levi, W. Handford, and W. Taylor, "Automated analog mixed signal IP generator for CMOS technologies," GOMATech 2019.	11	Co-Author	Government Conference	
J6	Y.-D. Jeon, **J.-W. Nam**, K.-D. Kim, T. M. Roh, and J.-K. Kwon, "A dual-channel pipelined ADC with sub-ADC based on flash–SAR architecture," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 59, no. 11, pp. 741–745, Nov. 2012.	5	Co-Author	SCIE (IF=1.327)	
J5	Y.-K. Cho, Y.-D. Jeon, **J.-W. Nam**, and J.-K. Kwon, "A 9-bit 80 MS/s successive approximation register analog-to-digital Converter with a capacitor reduction technique," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, no. 7, pp. 502–506, Jul. 2012.	4	Co-Author	SCIE (IF=1.327)	
J4	Y.-K. Cho, Y.-D. Jeon, **J.-W. Nam**, and J.-K. Kwon, "A 10-bit 30-MS/s successive approximation register analog-to-digital converter for low-power sub-sampling applications," Elsevier Microelectronics Journal, vol. 42, no. 12, pp. 1335–1342, Jul. 2011.	4	Co-Author	SCIE (IF=0.919)	
C4	**J.-W. Nam**, Y.-D. Jeon, S.-J. Yun, T. M. Roh, and J.-K. Kwon, "A 12-bit 100-MS/s pipelined ADC in 45-nm CMOS," in Proc. IEEE ISOCC, 2011, pp. 405–407.	5	First Author	International Conference	Poster Presentation
J3	**J.-W. Nam**, Y.-D. Jeon, Y.-K. Cho, J.-K. Kwon, "A 12-Bit 200-MS/s pipelined A/D converter with sampling skew reduction technique," *Elsevier Microelectronics Journal*, no. 11, vol. 42, pp. 1225-1230, Nov. 2011.	4	First Author	SCIE (IF=0.919)	
C3	Y.-D. Jeon, Y.-K. Cho, **J.-W. Nam**, W.-Y. Lee, K.-T. Hong, and J.-K. Kwon, "A 9.15mW 0.22mm^2 10b 204MS/s pipelined SAR ADC in 65nm CMOS," IEEE Custom Integrated Circuits Conf., Sep. 2010, pp. 1–4.	6	Co-Author	International Conference	Oral Presentation
C2	**J.-W. Nam**, Y.-D. Jeon, Y.-K. Cho, S.-G. Lee, and J.-K. Kwon, "A 2.85mW 0.12mm^2 1.0V 11-bit 20-MS/s algorithmic ADC in 65nm CMOS," in Proc. IEEE ESSCIRC, 2009, pp. 468–471.	5	First Author	International Conference	Oral Presentation
J2	Y.-D. Jeon, Y.-K. Cho, **J.-W. Nam**, S. -C, Lee, and J.-K. Kwon, "A 1.2 V 12 b 60 MS/s CMOS analog front-end for image signal processing applications," Elsevier ETRI Journal, vol. 31, no. 6, Dec. 2009.	5	Co-Author	SCIE (IF=1.159)	
J1	H. B. Le, **J.-W. Nam**, S.-T. Ryu, and S.-G. Lee, "Single-chip A/D converter for digital microphones with on-chip preamplifier and time-domain noise isolation," Electronics Letter, vol. 45, no. 3, pp. 151-153, 2009.	4	Co-Author	SCIE (IF=1.232)	
C1	H.-B. Le, **J.-W. Nam**, S.-T. Ryu, and S.-G. Lee, "A CMOS sigma-delta modulator for a digital electret microphone with a high input-impedance preamplifier," 15th Korean Conf. on Semiconductors, Phyeong-Chang, Feb. 2008.	4	Co-Author	Domestic Conference	Poster Presentation

b) Patents (ending Patents are excluded)

	Name of the Patent, Inventor, Registration No., Date of the Registration	# of Inventors	Participation Rate (%)	Country of Registration	
				South Korea	US
19	Multi-level PAM High-speed Transmitter, **Jaewon Nam**, Changwan Kim KR10-2021-0063714, May 17. 2021.	2	50	√	PCT
18	Apparatus and method for reducing a noise in an output waveform using a multi-bit sigma-delta modulator and a three-phase inverter, **Jaewon Nam**, Minki Kim, Jimin Oh, Yil suk Yang, KR101854395B1, May 8, 2018, US9350226B2, May 24, 2016.	4	40	√	√
17	Sensorless BLDC motor systems and driving methods of sensorless BLDC motor, Young Kyun Cho, Hui Dong Lee, **Jaewon Nam**, Jong-Kee Kwon, KR101803384B1, Nov. 30, 2017, US8836259B2, Sept. 16, 2014.	4	10	√	√

16	Triangular wave generator and method generating triangular wave thereof, Hui Dong Lee, **Jaewon Nam,** Young Kyun Cho, Jong-Kee Kwon, Yil suk Yang, Jongdae Kim, KR101801199B1, Nov. 24, 2017, US8604845B2, Dec. 10, 2013.	6	10	√	√
15	Motor control device and method of controlling the same, **Jaewon Nam**, Young Kyun Cho, Hui Dong Lee, Yil suk Yang, Jong-Kee Kwon, Jongdae Kim, KR101739911B1, May 26, 2017, US9490734B2, Nov. 8, 2016.	6	50	√	√
14	Pipelined analog digital convertor, **Jaewon Nam**, Young Deuk Jeon, Young Kyun Cho, Jong-Kee Kwon, US8564469B2, Oct 22, 2013.	4	40		√
13	Reference voltage supply circuit including a glitch remover, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US8547081B2, Oct. 1, 2013.	4	10		√
12	Successive approximation register analog-digital converter and method for operating the same, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, KR101309837B1, Sept. 23, 2013, US8164504B2, Apr. 24, 2012.	4	10	√	√
11	Analog digital converter, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US8531328B2, Sept 10, 2013.	4	10		√
10	Pipelined analog digital converter, **Jaewon Nam**, Young Deuk Jeon, Young Kyun Cho, Jong-Kee Kwon, US8508392B2, Aug 13, 2013.	4	70		√
9	Analog digital converting device, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, US8362938B2, Jan. 29, 2013.	4	10		√
8	Pipeline analog-to-digital converter, **Jaewon Nam**, Young Deuk Jeon, Young Kyun Cho, Jong-Kee Kwon, KR101224102B1, Jan. 21, 2013, US8164497B2, Apr 24, 2012.	4	70	√	√
7	Digital-to-analog converter, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, KR101201892B1, Nov. 16, 2012, US8059022B2, Nov. 15, 2011.	4	10	√	√
6	Read-out circuit with high input impedance, Minhung Cho, Yi Gyoung Kim, **Jaewon Nam,** Jong-Kee Kwon, KR101183986B1, Aug. 19, 2012, US8300850B2, Oct. 30, 2012.	4	5	√	√
5	Successive approximation register analog-digital converter and method of driving the same, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, KR101182402B1, Sept. 13, 2012.	4	10	√	
4	Band-gap reference voltage generator, Young Kyun Cho, Young Deuk Jeon, **Jaewon Nam**, Jong-Kee Kwon, US8058863B2, Nov. 15, 2011.	4	10		√
3	Multi-stage successive approximation register analog-to-digital converter and analog-to-digital converting method using the same, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US7999719B2, Aug 16, 2011.	4	10		√
2	Multi-stage dual successive approximation register analog-to-digital convertor and method of performing analog-to-digital conversion using the same, Young Deuk Jeon, Young Kyun Cho, **Jaewon Nam**, Jong-Kee Kwon, US7978117B2, July 12, 2011.	4	10		√
1	Method of algorithmic analog-to-digital conversion and algorithmic analog-to-digital converter, Seung-Chul Lee, **Jaewon Nam**, Young Deuk Jeon, Jong-Kee Kwon, US7705764B2, Apr 27, 2010.	4	30		√

V. Research Experiences

	Project Title	Program/grantor	Period	Total Expenses	Form of Participation	Note
P15	4-20GHz BW, <10K Noise Temperature, >50dB SFDR CMOS Controller for Superconducting and Spin Quantum Processor	National Research Foundation of Korea (NRF)	03/2025 – 02/2029	000 (4Y)	Participant (PI: Prof. Kim, J.)	in millions of KRW
P14	Greenhouse monitoring system Pilot R&D	Korea Forest	02/2025 – 06/2025	10 (4-month)	PI	
P13	12bit ADC Design	Silicon R&D	06/2024 – 02/2025	50 (6-month)	PI	
P12	Artificial Intelligence (AI) Semiconductor Human Resource Development (IITP-No.2024-0-00085)	IITP, Korea	07/2024 – 02/2025	000 (7M)	Participant (PI: Prof. Kim, Hyun)	
P11	Development of Image Sensor based on Monolithic Colloidal Quantum Dot Process	POSTECH (ADD Project)	03/2023 – 11/2025	184 (2.5Y)	PI	
P10	Development for Processing Software on AI Semiconductor Devices (IITP-2022-RS-2022-00156295)	IITP, Korea	07/2022 – 12/2029	7,500 (8Y)	Participant (PI: Prof. Lee, S.E.)	
P9	Next-Generation System Semiconductor Design Engineer Development Program (MOTIE-P0017011)	KIAT, Korea	03/2021 – 02/2026	5,900 (5Y)	Participant	
P8	Development of Cryogenic CMOS Interconnect Electronics for Large-Scale and Reliable Quantum Computer (BRL) (NRF-2022R1A4A3029433)	National Research Foundation of Korea (NRF)	06/2022 – 02/2025	500 (2.5Y)	Co-PI (PI: Prof. Kim, J.)	
P7	PCIe Gen 6.0 CMOS ADC based Receiver 2021R1G1A1003326	National Research Foundation of Korea (NRF)	03/2021 – 02/2024	30 /Year	PI	
P6	PUF Hardware security SoC Development (NRF) 2021R1A2C2005258	National Research Foundation of Korea (NRF)	03/2021 – 02/2026	250 /Year	Participant (PI: Prof. Hong, J.-P.)	
P5	POSH (Posh Open-Source Hardware) (FA8650-18-2-7853)	Defense Advanced Research Project Agency (DARPA), US	06/2018 – 08/2019	6	Participant	in millions of USD
P4	Multi-Tier Reconfigurable Transceivers for Hand-Portable Radios and Micro Base Stations in Networked Warfare (N00014-11-1-0819)	Office of Naval Research (ONR), US	08/2012 – 08/2016	3.25	Researcher	
P3	High Voltage/Current Power Module and ESD for BLDC Motor (MKE-10035171)	Ministry of Knowledge Economy (MKE), South Korea	03/2010 – 02/2015	1,675	Researcher (Supervision Institution)	in millions of KRW
P2	45nm Analog Circuit for Mixed-signal SoC (MKE-415106883)		03/2008 – 02/2010	1,365		
P1	Electrical components/module for ubiquitous terminal (MKE-415100592)		03/2006 – 02/2010	4,920		

VI. Invited Talks

	Organization	Host	Date	Location
1	Qualcomm Atheros (Topic: Embedded Passive gain SAR ADC)	Dr. Su, David	08/2013	San Jose, CA, US
2	Marvell Semiconductor Incorporation (Topic: ADC-based wireline receiver)	Dr. Gambhir, Manisha	10/2018	Santa Clara, CA, US
3	Georgia Tech, ECE (Faculty job interview) (Topic: Advanced High-speed ADC)	Dr. Wang, Hua	01/2019	Atlanta, GA, US

4	University of Washington Bothell, EE (Faculty job interview) (Topic: Advanced High-speed ADC)	Dr. Choi, Seungkeun	02/2019	Bothell, WA, US
5	Lawrence Berkeley National Laboratory (LBNL) (Job talk) (Topic: Low power ADC design technique)	Dr. Grace, Carl	05/2019	Berkeley, CA, US
6	Intel corporation (Job talk) (Topic: ADC-based wireline receiver)	Dr. O'mahony, Frank	06/2019	Hillsboro, OR, US
7	Dong-A University, ECE (Topic: GS/s ADC trends in high-speed transceiver)	Dr. Kim, Chang-Wan	10/2015	Pusan, South Korea
8	Electronics and Telecommunications Research Institute (Topic: 25Gbps High-speed PAM4 wireline transceiver)	Dr. Lee, Ja-Yol	10/2020	Daejeon, South Korea
9	The institute of Semiconductor Engineers (Topic: ADC-based wireline receiver)	ISE (Dr. Seung-eun Lee)	12/2020	Seoul, South Korea
10	ADC-based wireline receiver design	Dr. Jong-Phil Hong	02/2021	Chungju, South Korea
11	RF/Analog Workshop GS/s ADC Design Trends for the High-speed Links	Dr. Jae-Duk Han	09/2021	Seoul, South Korea

VII. Academic Mentoring Activities

	Topic	Student Name	Date	Current Affiliation (Title)
All Graduated Students (M.S. & Ph.D.)				
1	DDFS & Delta-sigma DAC design (Set-up Quantum Computer Electronics Project)	Park, Jae-Yun	2022 Summer ~ 2024.08	ADD, South Korea (Agency for Defense Development) SeoulTech (The 1st M.S. Student) *
2	CMOS Temperature Sensor & CIS ROIC 2023 Capstone design (Temperature Sensor) 2025 NRF Exchange student (KU Leuven & IMEC)	Yoo, Hyunyoung	2020 Winter ~ 2025.02	SeoulTech (The first B.S. student) * B.S. & M.S. Combined Program Ph.D. Program (2025 Spring ~)
3	PLL&DLL / AMS design automation in Python 2022 Capstone design (DLL)	Hyun, Jinwon	2022 Summer ~ 2025.02	LIG-Nex1 Dept. R&D (2025 Mar. ~)
4	Photodiode in Standard CMOS process & ADC 2022 Capstone design Winner (DC-DC Converter)	Kim, Dana	2021 Winter ~ 2025.02	LIG-Nex1 Dept. R&D (2025 Mar. ~)
5	SRAM based PUF design & BIST design 2022 Capstone design Winner (DC-DC Converter)	Yoo, Jimin	2021 Spring ~ 2025.02	Samsung Electronics (2025 March~) Dept. Foundry
6	LDO & Bandgap Reference circuit design 2022 Capstone design Winner (DC-DC Converter)	Lee, Hyun Jeong	2021 Spring ~	SeoulTech B.S. & M.S. Combined Program **(Dropped at the 3rd Semester)**
7	Incremental/Zoom/Domino ADC design 2023 Capstone design (Sigma-Delta ADC)	Kim, Su-hyeon	2022 Summer ~	SeoulTech B.S. & M.S. Combined Program M.S. Program (start 2024 Spring)
8	CMOS CIS ROIC (Ramp generator design) 2023 Capstone design (Recognized Award)	Kim, Yeon-Su	2022 Summer ~	SeoulTech B.S. & M.S. Combined Program M.S. Program (2024 Spring ~)
9	SRAM based PUF & ECC 2023 Capstone Design (Winner) 2024 IEEE Paper Contest (Silver Award @ Seoul)	Yu, Kwangmin	2022 Fall ~	SeoulTech M.S. Program (2024 Spring ~)
10	RF Component (Transformer & Inductor) Design 2024 Capstone design (Winner with Song, C.-Y.)	Yoo, Eunji	2023 Fall ~	B.S. & M.S. Combined Program
11	Cryo-CMOS Circuit Design	Ro, Kwangpyo	2024 Fall ~	M.S. Program **(Dropped at the 2nd Semester)**
12	CIS & SPAD ROIC Design & Device Modeling	Jeon, Myeong-Hyun	2024 Fall ~	M.S. Program (2024 Fall ~)
13	Inductor Modeling & Cryo-CMOS Circuit Design	Yoo, Eunji	2003 Fall ~	M.S. Program (2025 Spring ~)
Qualified Undergraduate Students (B.S.)				
1	High-speed PRBS generator design in 65nm	Lim, Si-Young	2020-2021	Hynix, South Korea (The first B.S. Student) *
2	CMOS VLSI EDA tutoring	Lee, Ji-hun	2021 Summer	KU-KIST M.S. Program

3	Wideband Amp & Active Inductor design 2022 Capstone (DC-DC Converter)	Lee, Hae-Chan	2021 Summer	Samsung DS (Memory Dept.) Intern Samsung Electronics, Dept. Memory
4	UWB Channel Selection Filter design	Kim, Won-Jun Park, Narin	2022 (1-Year)	SeoulTech 2022 Capstone Design
5	SRAM-based PUF SoC	Seungbum Baek	Ph.D. Defense Committee	Samsung Electronics (PUF Design Team)
6	Delay-Locked Loop for high-speed link	Kim, Jae-Yoon	2022 (1-Year)	SeoulTech 2022 Capstone Design LG Electronics
7	Optimizing EV Chargers Location via Integer Programming	Choi, Youlim, Im, Sunghyun, Jung Hansoo	2023 (1-Year)	SeoulTech 2023 Capstone Design
8	Dickson Charge Pump Design in ETRI 500nm 2024 Capstone Design Winner (with Yoo, Eunji)	Song, Chae-Yoon	2023 (2-Year)	SeoulTech B.S. Intern (AD-Lab) SeoulTech 2023 Capstone Design
9	Mixed Signal Circuits and Systems Design (ASIC Layout Engineering) 2024 IITP AI-ON Design contest Winner	Lee, Guhyeon	2024 Spring ~	SeoulTech B.S. Intern (AD-Lab)
10	Mixed Signal Circuits and Systems Design (ASIC Layout Engineering) 2024 IITP AI-ON Design contest Winner	Lee, Si-Hyung	2024 Spring ~	SeoulTech B.S. Intern (AD-Lab)
11	Mixed Signal Circuits and Systems Design (ASIC Layout Engineering & Testing PUF) 2024 IITP AI-ON Design contest Winner	Jeong Woojin	2024 Spring ~	SeoulTech B.S. Intern (AD-Lab)
12	QCRX ADC design 2025 Capstone (Greenhouse monitoring H/W)	Jang, Inkwon	2024 Winter ~	SeoulTech B.S. Intern (AD-Lab)
13	2025 Capstone (Greenhouse monitoring S/W)	Jeong, Howon	2025 Spring ~	SeoulTech B.S. Intern (AD-Lab)
14	2025 Capstone (Greenhouse monitoring S/W)	Choi, Sua	2025 Spring ~	SeoulTech B.S. Intern (AD-Lab)
15	RF Transmitter (with Prof. Choi, Kyung-Sik)	Park, Sanggyu	2025 Spring ~	SeoulTech B.S. Intern (STAN-Lab) SeoulTech B.S. Intern (AD-Lab)
16	RF Transmitter (with Prof. Choi, Kyung-Sik)	Jung, Seuk	2025 Spring ~	SeoulTech B.S. Intern (STAN-Lab) SeoulTech B.S. Intern (AD-Lab)
Mentoring Activities Before join SeoulTech				
1	Analog-front-end circuits design (M.S. Direct Research at Dr. Chen's group, USC)	Park, Jong	2014 Fall	LG Electronics, Korea (Specialist at LG-CTO), Samsung Electronics, Korea (Dept. of LSI since 2021)
2	High resolution ADC Design in 14nm FinFET (M.S. Direct Research at Dr. Chen's group)	Ravindranath, Abhilash	2017 Spring	Ansys, Inc., US (Senior Application Engineer)
3	Mixed-signal integrated circuits for a testing (M.S. Direct Research at Dr. Chen's group)	Zhou, Ruohan	2017 Fall	Western Digital, US (Senior Engineer)
4	CMOS VLSI EDA tutoring	Dr. Park, Soowang	2018 Fall	Apple, US (ASIC Design Engineer)
5	CMOS circuit design and testing (USC-KAU Summer intern program)	Kwon, O-Sung	2019 Summer	Samsung Electronics, Korea